mmTron
Unleashing the mmWave Frontier

TMC163-D
DC-20 GHz Distributed High Linearity Amplifier

Product Features

- RF frequency: DC to 20 GHz
- Linear Gain: 17 dB
- Noise Figure: 2.5 dB
- Die Size: X=3 mm, Y=1.55 mm, Z=0.1mm
- DC Power: 8 VDC, 180 mA

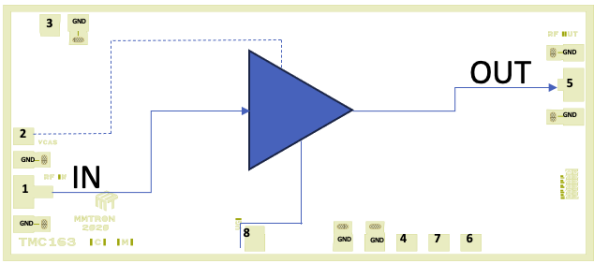
Applications

- Point-to-Point Radios and VSATs
- Test instrumentation
- Fiber Optics
- Military, EW and Space

Product Description

The TMC163D GaAs PHEMT Distributed amplifier is a broadband Ultra High Linearity device, designed for use in Radios, Test instrumentation, Military, EW and Space applications. The TMC163D is a 50 W matched design providing 34dBm of OIP3 and eliminates the need for RF port matching. The typical bias for TMC163D is 8V and 180mA but it can be biased to as low as 5V and 140mA with excellent performance. Both bond pad and backside metallization are Au-based that is compatible with ribbon and wedge bonding and high conductivity epoxy and eutectic die attach methods.

Functional Block Diagram



*Input and Output RF signals are AC coupled (need to add blocking capacitors)

Ordering Information

Part No.	Description
TMC163D	Bare Die[1]

1- See Assembly Techniques for die attach options

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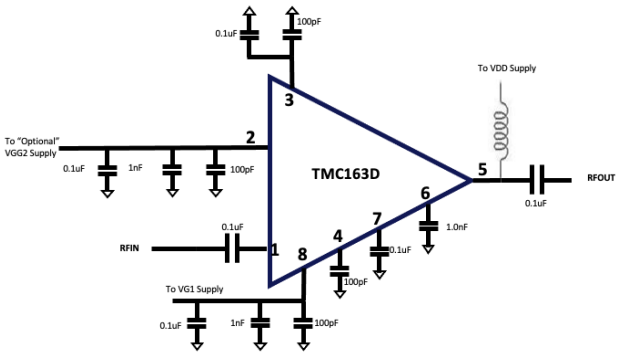
Typical Operating Conditions

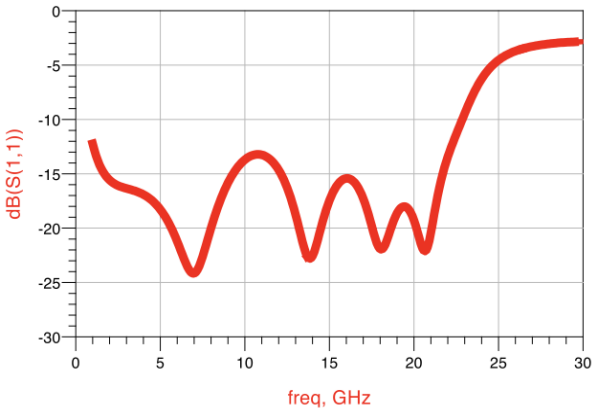
	Min	Typ	Max	
Frequency	DC		20	GHz
Gain		17		dB
P1dB		26		dBm
Psat		27		dBm
Noise Figure		3		dB
OIP3		34		dBm
Bias Voltage		8		V
Bias Current		180		mA

* Electrical Performance : Vdd = 8 V, VGG = -0.6 V, TA = 25 °C, F=20 GHz

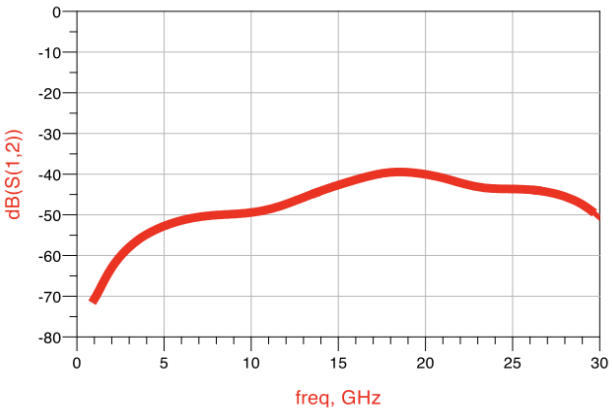
Application Circuit TMC163



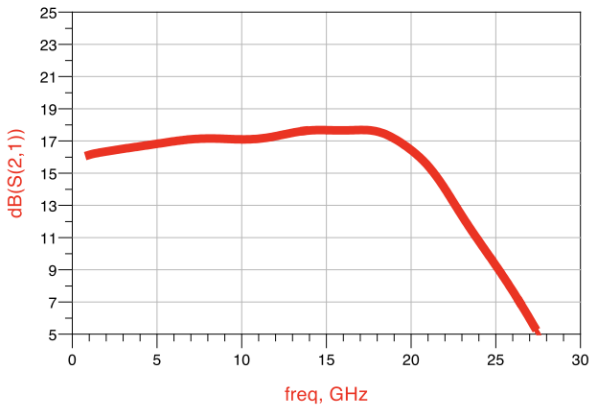
TMC163 Input Return Loss



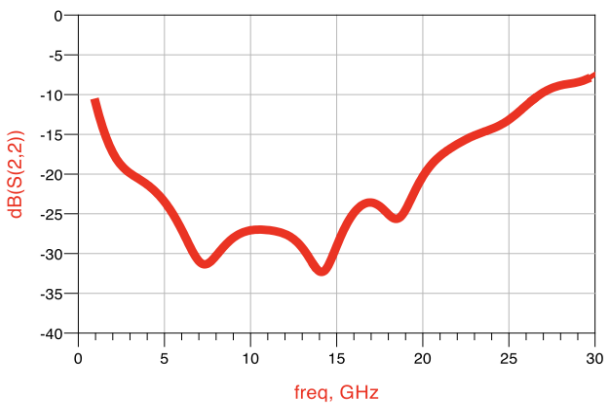
TMC163 Reverse Isolation



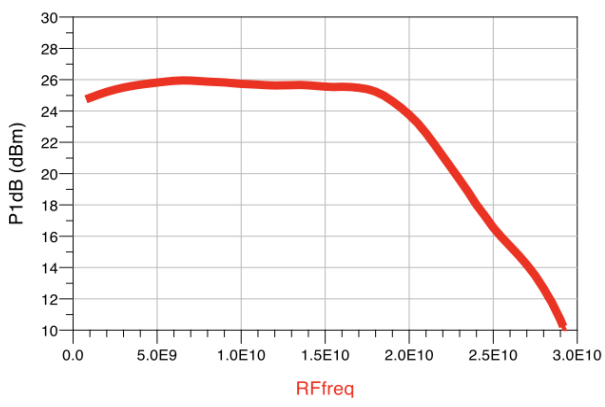
TMC163 Gain



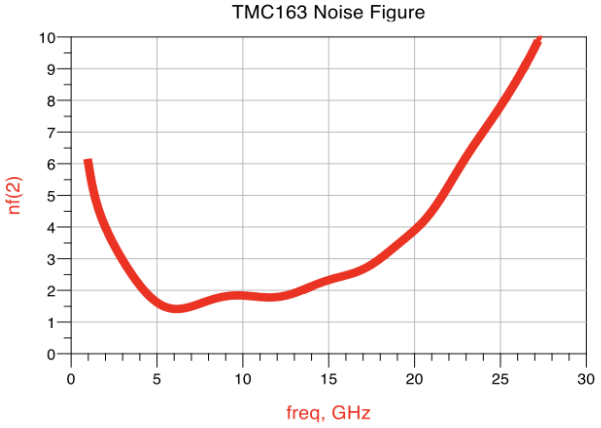
TMC163 Output Return Loss



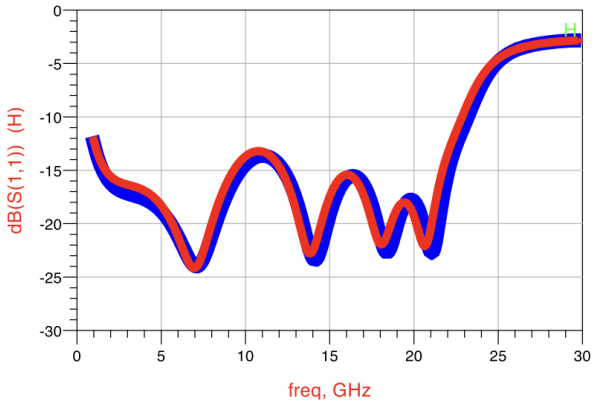
TMC163 P1dB



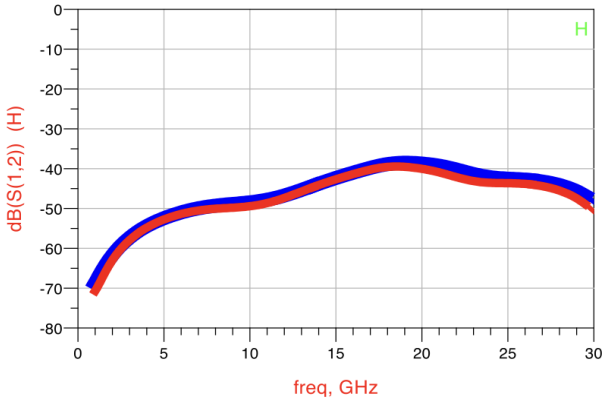
TMC163 Noise Figure



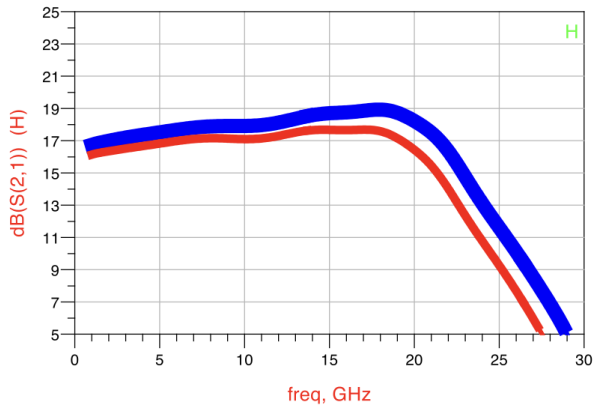
TMC163 Input Return Loss



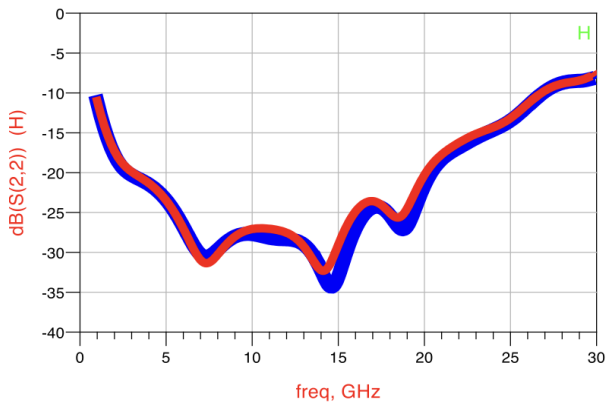
TMC163 Reverse Isolation



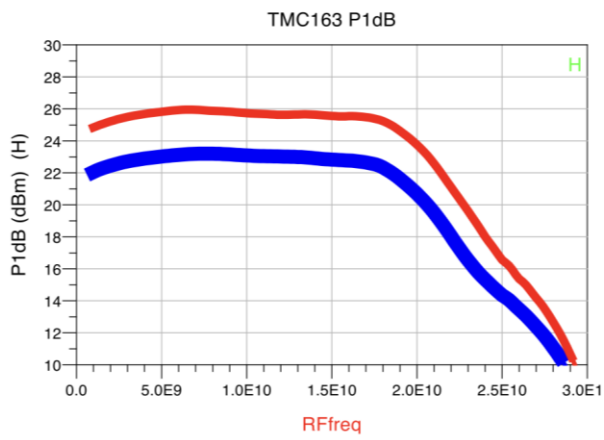
TMC163 Gain



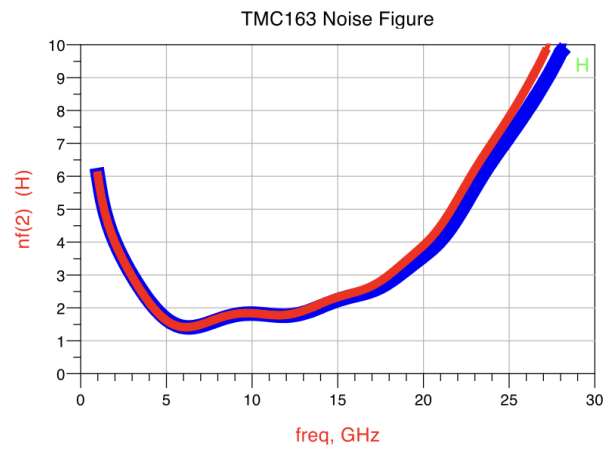
TMC163 Output Return Loss



TMC163 P1dB

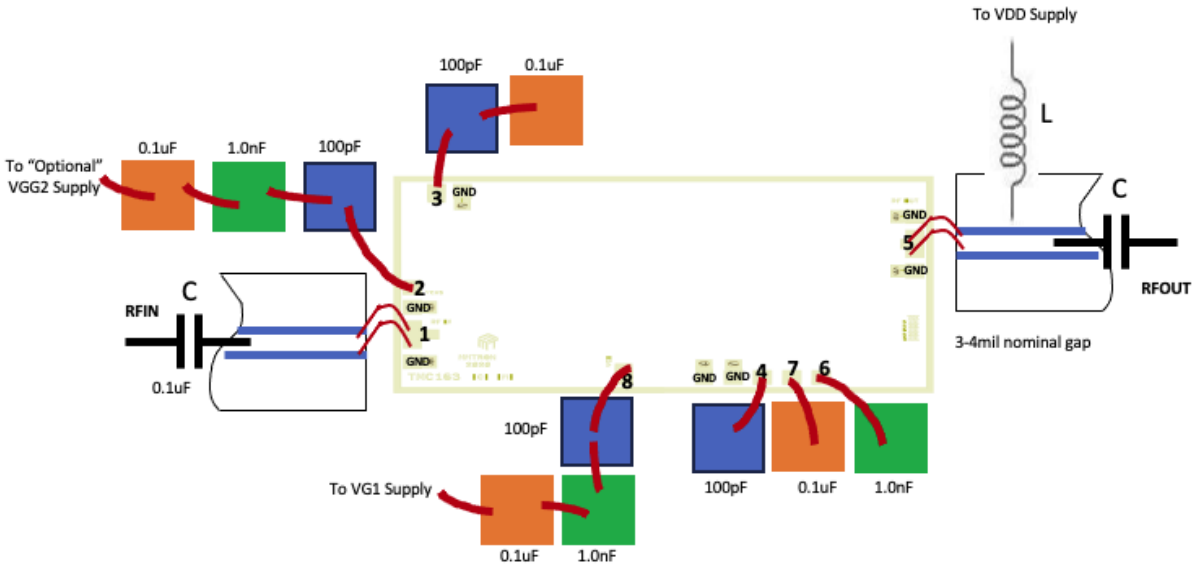


TMC163 Noise Figure

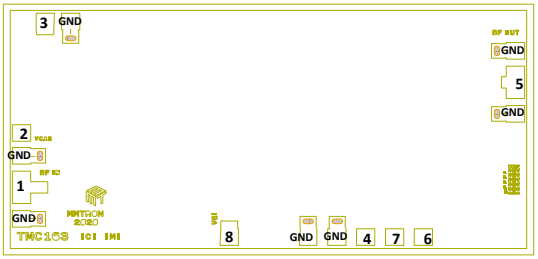


Red Curve is for 8V/180mA Bias, and Blue curve is for 5V/180mA bias.

Assembly Drawing



Bare Die Layout Drawing and Functional Description



Recommended Biasing

The TMC163D is operated with one positive supply VDD and one negative supply voltage VGG. The positive supply must be connected to the output pad through a bias-T. The negative voltage VGG should be connected to VG1 pad on the die. The VGG is biased to -1V first, then VDD is gradually biased to +8V and finally, VG1 is adjusted to around -0.6V for IDD=530mA DC current.

Reverse the sequence during power down, i.e. bring the VGG to -1V, lower VDD to 0V, and then VGG to 0.

Pad #	Function	Description
1	RF INPUT	This pad is DC coupled and matched to 50 Ohms. Blocking capacitor is required.
2	VGG2 (VCAS)	Gate 2 for amplifier. Attach 100pF/0.01uF chip bypass capacitors. Typical operation has VGG2(VCAS) biased internal to IC. Setting VGG2 externally can be used to adjust NF, Gain and OIP3.
3	ACG1	Low frequency termination. Attach 100pF/0.1uF chip bypass capacitor.
4	ACG2	Low frequency termination. Attach 100 pF chip bypass capacitor.
5	RF OUTPUT & VDD	RF output for amplifier. Connect DC bias (Vdd) network to provide drain current (Idd).
6	ACG3	Low frequency termination. Attach 1 nF chip bypass capacitors.
7	ACG4	Low frequency termination. Attach 100pF/0.1uF chip bypass capacitor.
8	VGG1 Bias	Gate control 1 for amplifier. Attach 100pF/1nF/0.1uF bypass capacitors.

Recommended Biasing

The TMC163D is fabricated using a GaAs-based semiconductor material structure. All bare die are placed in Gel based ESD protective containers, and then sealed in an ESD protective bag for shipment. Once the sealed ESD protective bag has been opened, all die should be stored in a humidity-controlled dry nitrogen environment.

Use a vacuum collet sized to handle the chip along the edges to avoid touching the air bridges. The die is back-metalized and can be mounted with standard AuSn eutectic or conductive epoxy assembly techniques. The mounting surface should be clean and flat.

Assembly Techniques

Eutectic Die Attach:

The most common eutectic alloy used in die attach is the gold-tin (AuSn) alloy. With a melting point of 280°C, it provides a strong, reliable bond without requiring excessively high temperatures that could potentially damage the die or the substrate. Eutectic die attach is generally performed in a two-step process. First, the eutectic alloy is deposited onto the die or substrate, often by a process such as electroplating or sputtering. This forms what is known as the "preform". Next, the die is placed onto the preform, and the assembly is heated to the melting point of the alloy. This causes the alloy to reflow, spreading out to cover the entire interface between the die and the substrate. Once cooled, the alloy solidifies, creating a robust bond between the die and the substrate. A 80/20 AuSn preform with a work surface temperature of 255 °C is recommended. The tool temperature of 265 °C should be used. The chip should not be exposed to a temperature greater than 300 °C for more than 45 seconds. A maximum 3 seconds of scrubbing should be sufficient for die attachment.

Epoxy Die Attach:

Apply a minimum amount of epoxy such as Ablestick 84-1LMI m(0.25-0.75mil) to the mounting surface so that a thin epoxy fillet is observed around the perimeter of the chip once it is placed into position. Cure epoxy per the manufacturer's schedule. The epoxy fillet around the die should be approximately half-way up the side of the 4-mil thick MMIC. Too little epoxy may lead to voids, too much epoxy may lead to stringers and shorts to the front-side metal.

Wire Bonding:

RF wedge bonds made with two 1 mil wires are recommended for RF ports. A single 1mil wire can be used for DC pads. Ensure the bonding tool is grounded. These bonds could be bonded thermosonically with a force of 50 grams and a stage temperature of 150 °C. Use a shim under the die to bring the top surface of the die level with the RF input and output transmission line to

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Absolute Maximum Ratings

Parameter	Value / Range
Drain Bias Voltage (VDD)	+10 V
Gate Bias Voltage (VG1)	-2 to 0 V
Gate Bias Current (IG1)	+5 mA
RF Input Power (RFIN) (VDD=+8V)	+24 dBm
Channel Temperature	175 °C
Continuous Pdiss, (T=85°C) (derate 40 mW/°C above 85 °C)	4.3 W
Thermal Resistance (channel to die bottom)	20.8 °C/W
Storage Temperature	-65 to +150 °C
Operating Temperature for MTTF>1E6 hrs.	-55 to +125 °C



Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. mmTron Inc. recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications. III-V MMICs are ESD-sensitive. Preventative ESD measures must be employed in all aspects of storage, handling, and assembly. MMIC ESD precautions, handling considerations, and die-attach and bonding methods are critical factors in successful III-V MMIC performance and reliability.



RoHS Compliant

This part is RoHS compliant, meeting the requirements of the EU Restriction of Hazardous Substances Directive 2002/95/EC, commonly known as RoHS. Six substances are regulated: lead, mercury, cadmium, chromium VI (hexavalent chromium), polybrominated biphenyls (PBB), and polybrominated biphenyl ethers (PBDE). RoHS compliance requires that any residual concentration of these substances is below the Directive's maximum concentration values (MCV): cadmium 100ppm by weight and all others 1000ppm by weight.

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