

## Product Features

- RF frequency: 3 to 16 GHz
- Linear Gain: 16 dB
- OIP3: 29 dBm
- PKG Size: X=7 mm, Y=7mm, Z=0.8 mm
- DC Power: 5 VDC, 250 mA

## Application

- Instrumentation
- 5G Wireless
- SATCOM
- Military Radar, EW

## Product Description

The TMC161 ADC interface low noise quasi differential amplifier consists of a differential anti-alias filter, a pair of quasi differential distributed low noise amplifiers and designed to be integrated with a balun packaged in an air-cavity QFN. TMC161 is designed for use in 5G wireless, SATCOM, Instrumentation and Military Radar and EW applications. The TMC161 is a 50 Ω matched design with built-in bias-T which eliminates the need for RF port matching and external bias-T. To ensure rugged and reliable operation and moisture protection, the TMC161 is designed and layed out for maximum reliability. Both bond pad and backside metallization are Au-based that is compatible with ribbon and wedge bonding and high conductivity epoxy and eutectic die attach methods. The anti-alias filter can be custom designed to reject clock frequency and its mixing components.

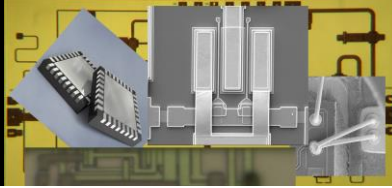
### *Electrical Performance : Vdd = 5 V, Vgg = -0.7 V, TA = 25 °C*

	min	Typ	Max	Units
<b>Frequency</b>	3		16	GHz
<b>Gain</b>		16		dB
<b>Noise Figure</b>		6		dB
<b>OIP3</b>		29		dBm
<b>Return Loss</b>		10		dB
<b>Bias Voltage</b>		5		V
<b>Bias Current</b>		250		mA

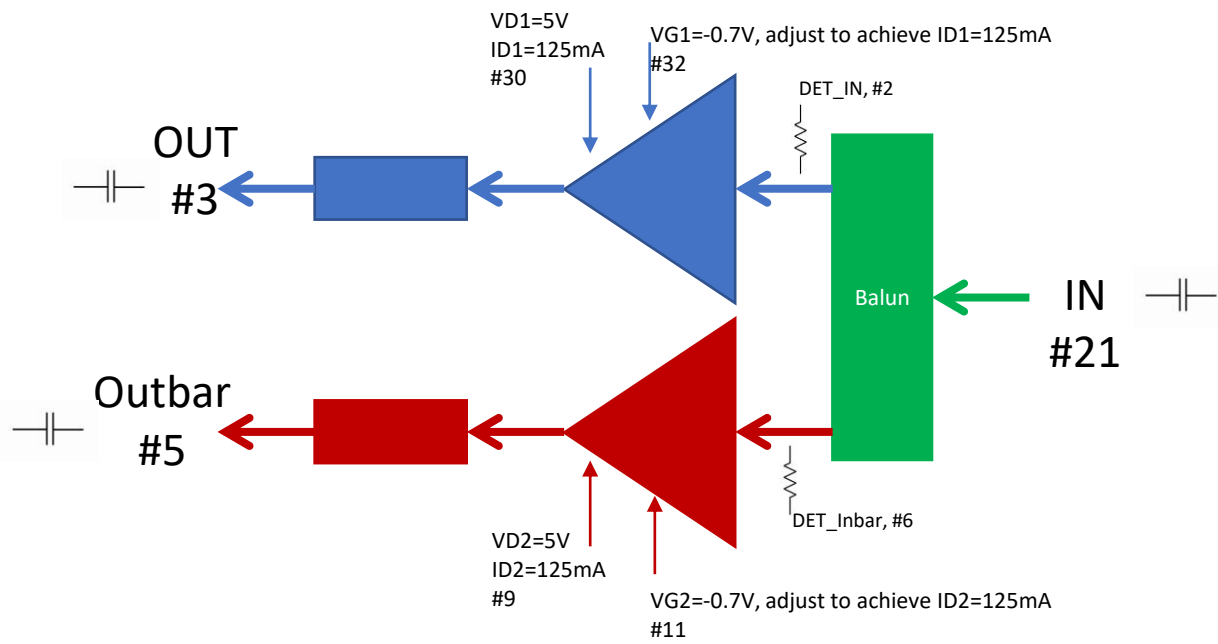
# TMC161

## 3-16 GHz

### ADC Interface IC



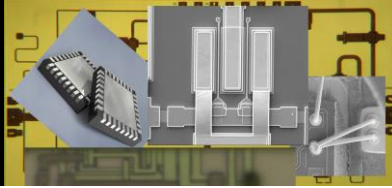
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**Bias Sequencing:** To turn ON the device, VG1, and VG2 are first set at -1V. Then set VD1 and VD2 to 5V. Finally, adjust VG1 and VG2 to achieve ID1=ID2=125mA. To turn OFF the device, you set VG1 and VG2 to -1V, then turn off the VD1 and VD2 followed by turning off VG1 and VG2.

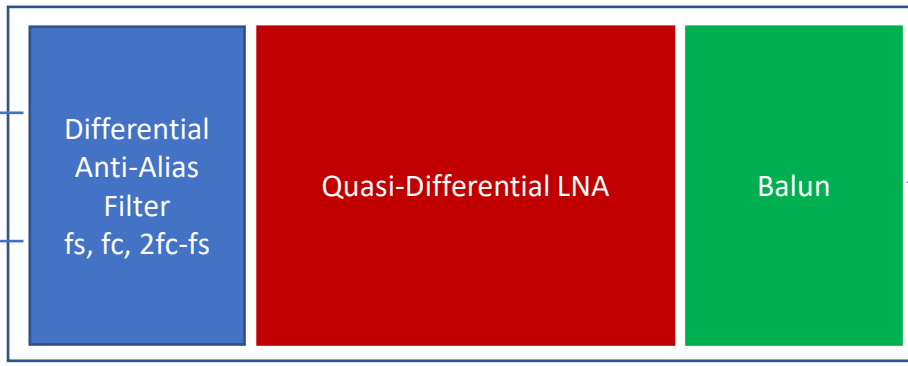
Pad #	Function	Pad #	Function	Pad #	Function
2	Input Detector Voltage	9	VDD BIAS (Input bar)	22	GND
3	Input	11	VGG BIAS (Input bar)	28	VCAD BIAS (Input)
4	GND	13	VCAD BIAS (Input bar)	30	VGG BIAS (Input)
5	Input bar	20	GND	32	VDD BIAS (Input)
6	Input bar Detector Voltage	21	Output		

# TMC161 3-16 GHz ADC Interface IC

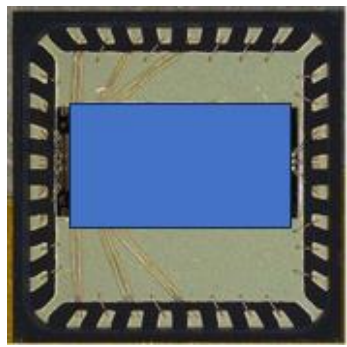


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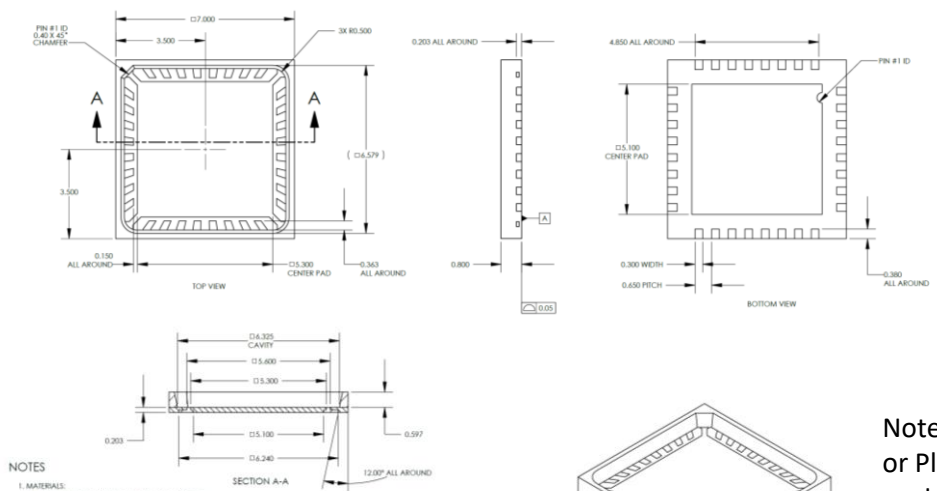
Differential  
Output  
Signals  
to ADC



Single-ended  
Input RF Signal



Input and output signals are DC coupled (need to add blocking capacitors)



- NOTES**
1. MATERIALS:  
LEAD FRAME: COPPER 1%MIN, THK = 0.203±0.009  
BODY: SEMICONDUCTOR MOLDING EPOXY. CONTACT QTECHNOLOGIES FOR DETAILS.
  2. FINISH:  
LEAD FRAME: ELECTROLESS NICKEL PER MIL-C-20274, CLASS 1,  
200 TO 300 MICROINCHES (2.5um-7.6um) THICK  
GOLDED PLAYS PER MIL-C-45204, TYPE 3, GRADE A, CLASS 1  
(60 TO 80 MICROINCHES (1.5um-2um) THICK)  
BODY SURFACE FINISH: VISA 21-24 (1.12-1.8um)
  3. PACKAGE MISMATCH: BODY OFFSET FOR LEAD FRAME = 0.076mm MAX.
  4. UNLESS OTHERWISE SPECIFIED, RADII ON ALL MOLDED EDGES  
AND CORNERS = 0.25mm MAX.
  5. PACKAGE CONFORMS TO JEDEC MO-220

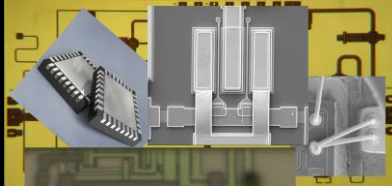


Note: Ceramic Air-cavity  
or Plastic Overmold  
package options are  
also available

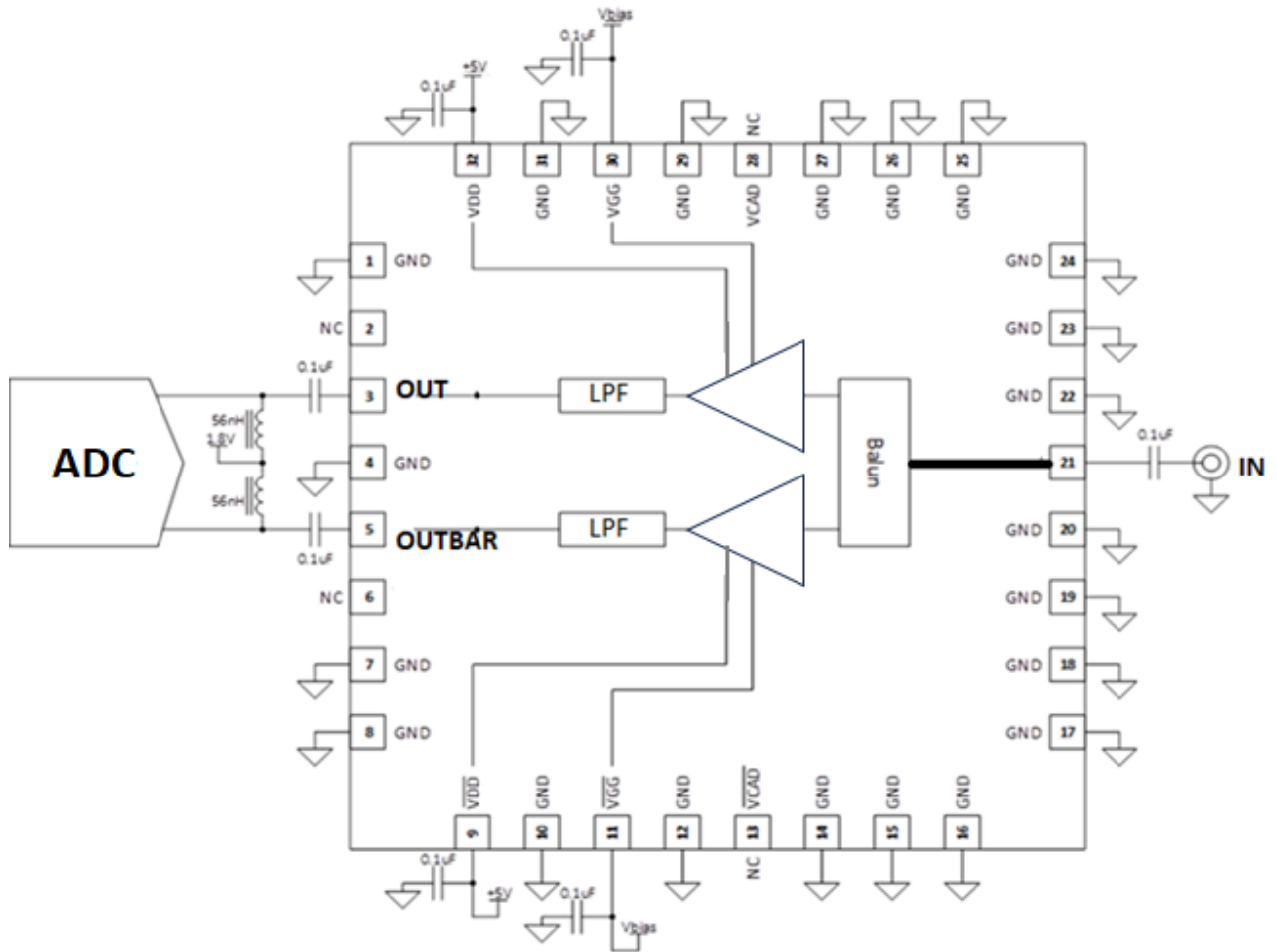
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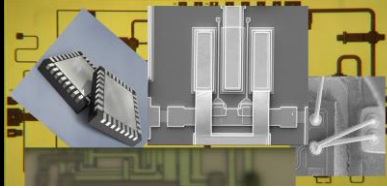
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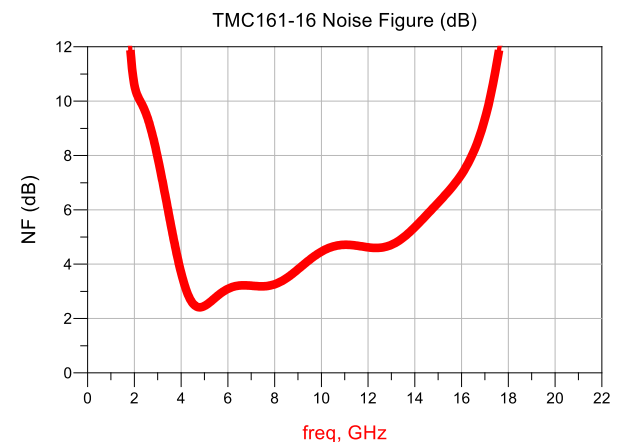
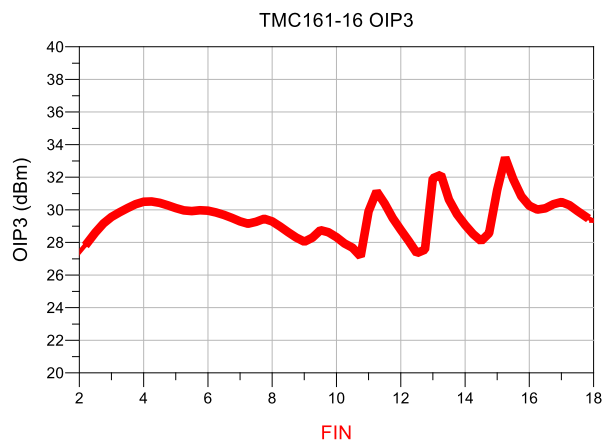
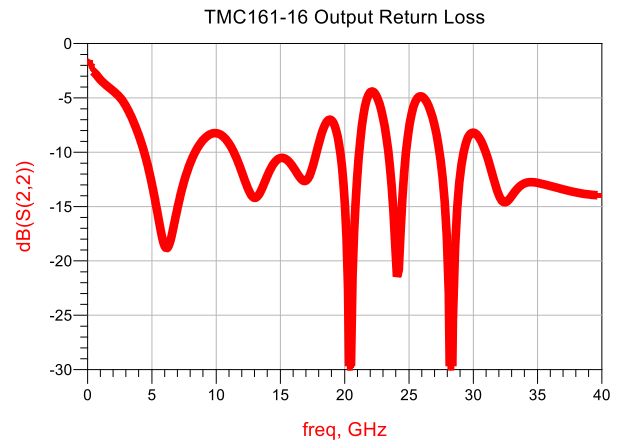
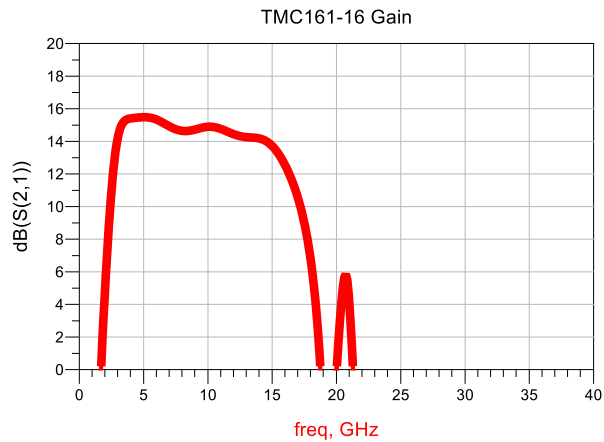
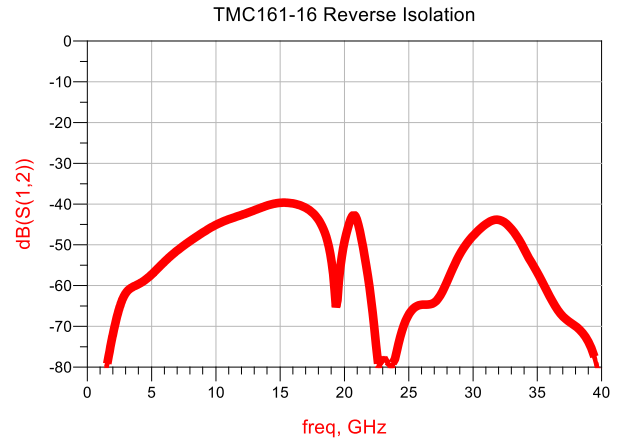
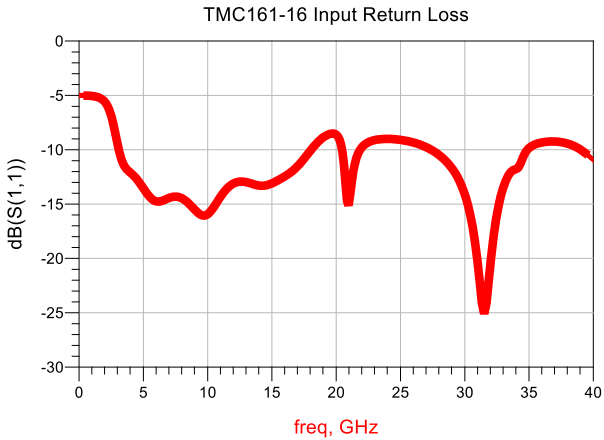
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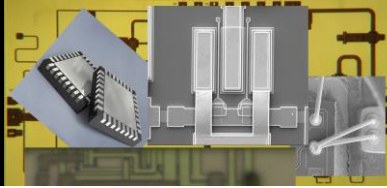
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### ADC Interface IC



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## • Recommended Biasing

- The TMC161 is operated with one positive supply VDD (VD1=VD2) and one negative supply voltage VGG (VG1=VG2). The positive supply must be connected to VD1 and VD2 pads on the package. The negative voltage VGG should be connected to VG1 and VG2 pads on the package. The VGG is biased to -1V first, then VDD is gradually biased to +5V and finally, VG1 and Vg2 are adjusted to around -0.7V for ID1=ID2=125mA DC current.
- Reverse the sequence during power down, i.e. bring the VGG to -1V, lower VDD to 0V, and then VGG to 0.

## • Assembly Techniques

- The TMC161 is fabricated using a GaAs-based semiconductor material structure and is to be packaged in an air-cavity QFN. The package is back-metalized and can be mounted with standard PCB assembly techniques. The mounting surface should be clean and flat.

## • ESD Warning

- III-V MMICs are ESD-sensitive. Preventative ESD measures must be employed in all aspects of storage, handling, and assembly. MMIC ESD precautions, handling considerations, and die-attach and bonding methods are critical factors in successful III-V MMIC performance and reliability.

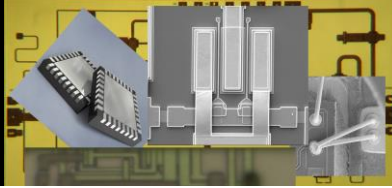
## • RoHS Compliance

- This part is RoHS compliant, meeting the requirements of the EU Restriction of Hazardous Substances Directive 2002/95/EC, commonly known as RoHS. Six substances are regulated: lead, mercury, cadmium, chromium VI (hexavalent chromium), polybrominated biphenyls (PBB), and polybrominated biphenyl ethers (PBDE). RoHS compliance requires that any residual concentration of these substances is below the Directive's maximum concentration values (MCV): cadmium 100ppm by weight and all others 1000ppm by weight.

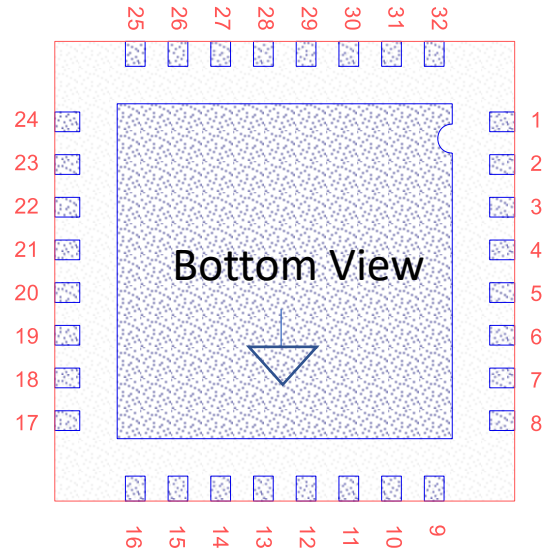
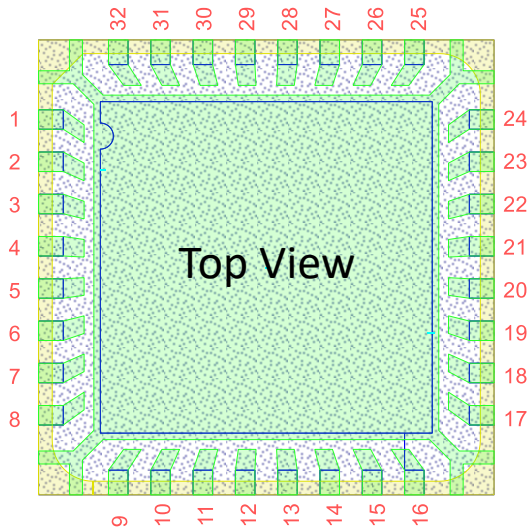
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Pad #	Function
2	NC
3	Output
4	GND
5	Output bar
6	NC

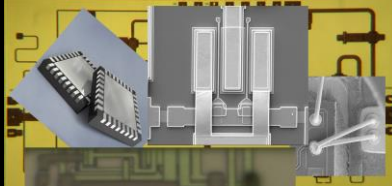
Pad #	Function
9	VDD BIAS (Output bar)
11	VGG BIAS (Output bar)
13	VCAD BIAS (Output bar)
20	GND
21	Input

Pad #	Function
22	GND
28	VCAD BIAS (Output)
30	VGG BIAS (Output)
32	VDD BIAS (Output)

Leave pins 13 and 28 are internally biased. Leave them open for normal operation. They can be biased externally for fine-tuning the performance.

Input and outputs are DC coupled. DC blocking caps are needed, Choose values to adjust the low-frequency end.

Connect all other pins to GND.



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