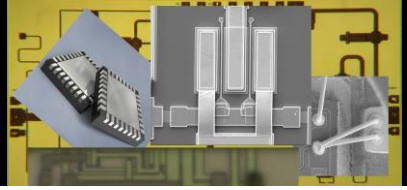
TMC160-16
3-16 GHz
DAC Interface IC



mmTRON
Unleashing the mmWave Frontier

Product Features

- RF frequency: 3 to 16 GHz
- Linear Gain: 16 dB
- OIP3: 29 dBm
- PKG Size: X=7 mm, Y=7 mm, Z=0.8 mm
- DC Power: 5 VDC, 250 mA

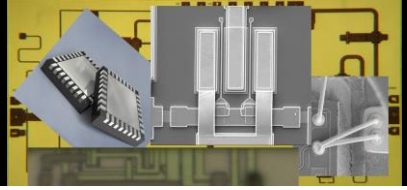
Application

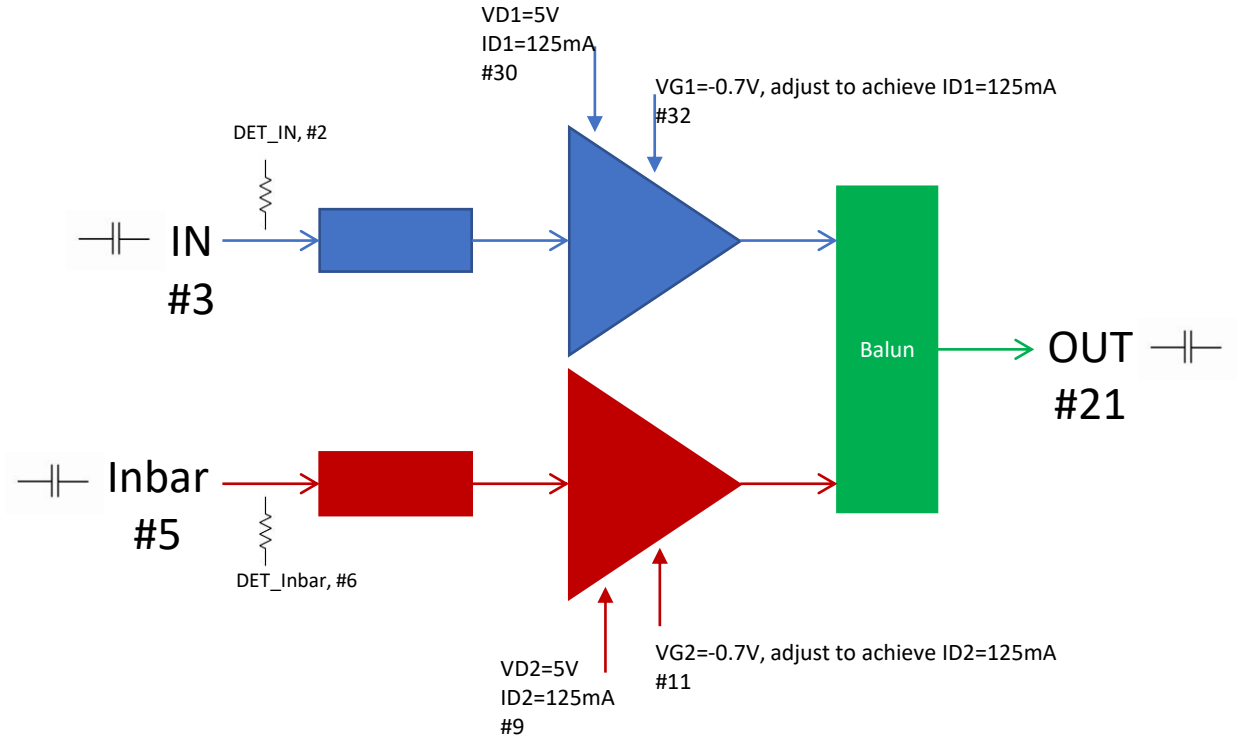
- Software-Defined Radio
- Instrumentation
- 5G Wireless
- SATCOM
- Military Radar, EW

Product Description

The TMC160-16 DAC interface low noise quasi differential amplifier consists of a differential anti-alias filter, a pair of quasi differential distributed low noise amplifiers and designed to be integrated with a balun packaged in an air-cavity QFN. TMC160-16 is designed for use in 5G wireless, SATCOM, Instrumentation and Military Radar and EW applications. The TMC160-16 is a 50 Ω matched design with built-in bias-T which eliminates the need for RF port matching and external bias-T. TMC160-16 can be biased from 5V to 8V and from 125mA to 160mA to optimize Noise Figure and Linearity for a variety of applications. To ensure rugged and reliable operation and moisture protection, the TMC160-16 is designed and layed out for maximum reliability. Both bond pad and backside metallization are Au-based that is compatible with ribbon and wedge bonding and high conductivity epoxy and eutectic die attach methods.
The anti-alias filter can be custom designed to reject clock frequency and its mixing components.

Electrical Performance : **Vdd = 5 V, Vgg = -0.7 V, TA = 25 °C**				
	min	**Typ**	**Max**	**Units**
Frequency	3		16	GHz
Gain		16		dB
Noise Figure		4		dB
OIP3		29		dBm
Return Loss		10		dB
Bias Voltage		5		V
Bias Current		250		mA



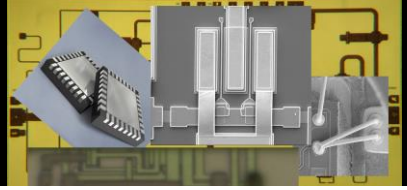


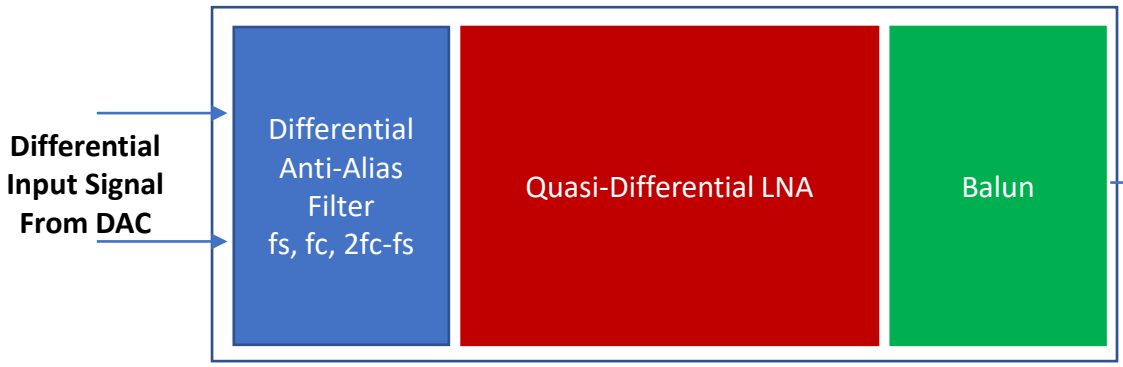
Bias Sequencing: To turn ON the device, VG1, and VG2 are first set at -1V. Then set VD1 and VD2 to 5V. Finally, adjust VG1 and VG2 to achieve ID1=ID2=125mA. To turn OFF the device, you set VG1 and VG2 to -1V, then turn off the VD1 and VD2 followed by turning off VG1 and VG2.

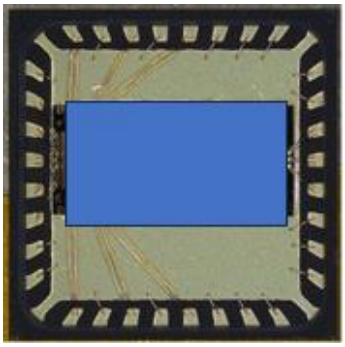
Pad #	Function
2	Input Detector Voltage
3	Input
4	GND
5	Input bar
6	Input bar Detector Voltage

Pad #	Function
9	VDD BIAS (Input bar)
11	VGG BIAS (Input bar)
13	VCAD BIAS (Input bar)
20	GND
21	Output

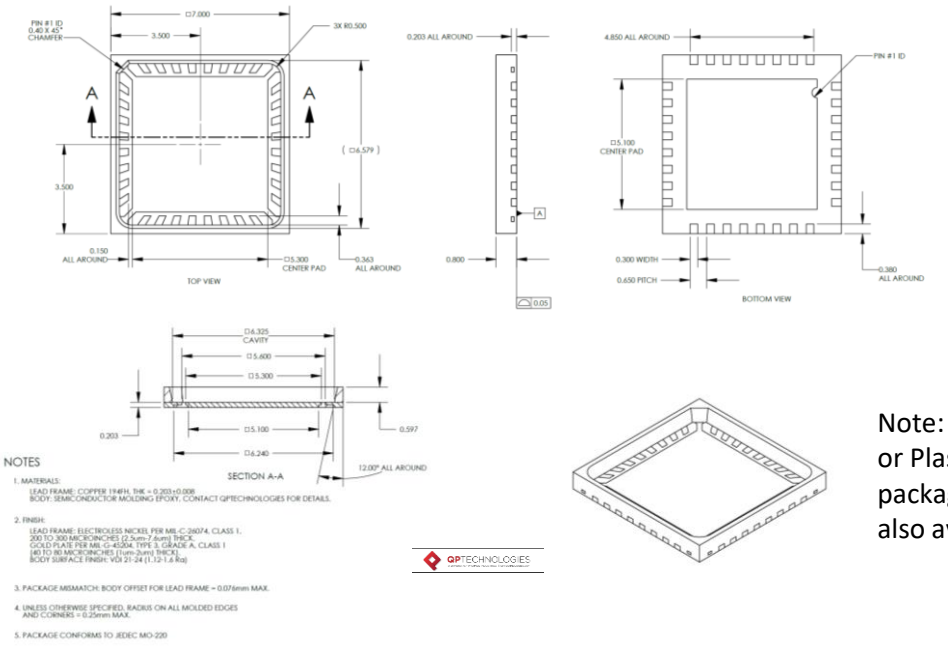
Pad #	Function
22	GND
28	VCAD BIAS (Input)
30	VGG BIAS (Input)
32	VDD BIAS (Input)



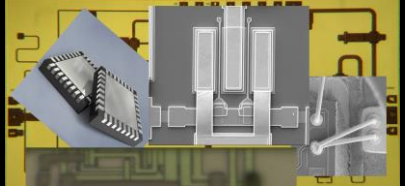


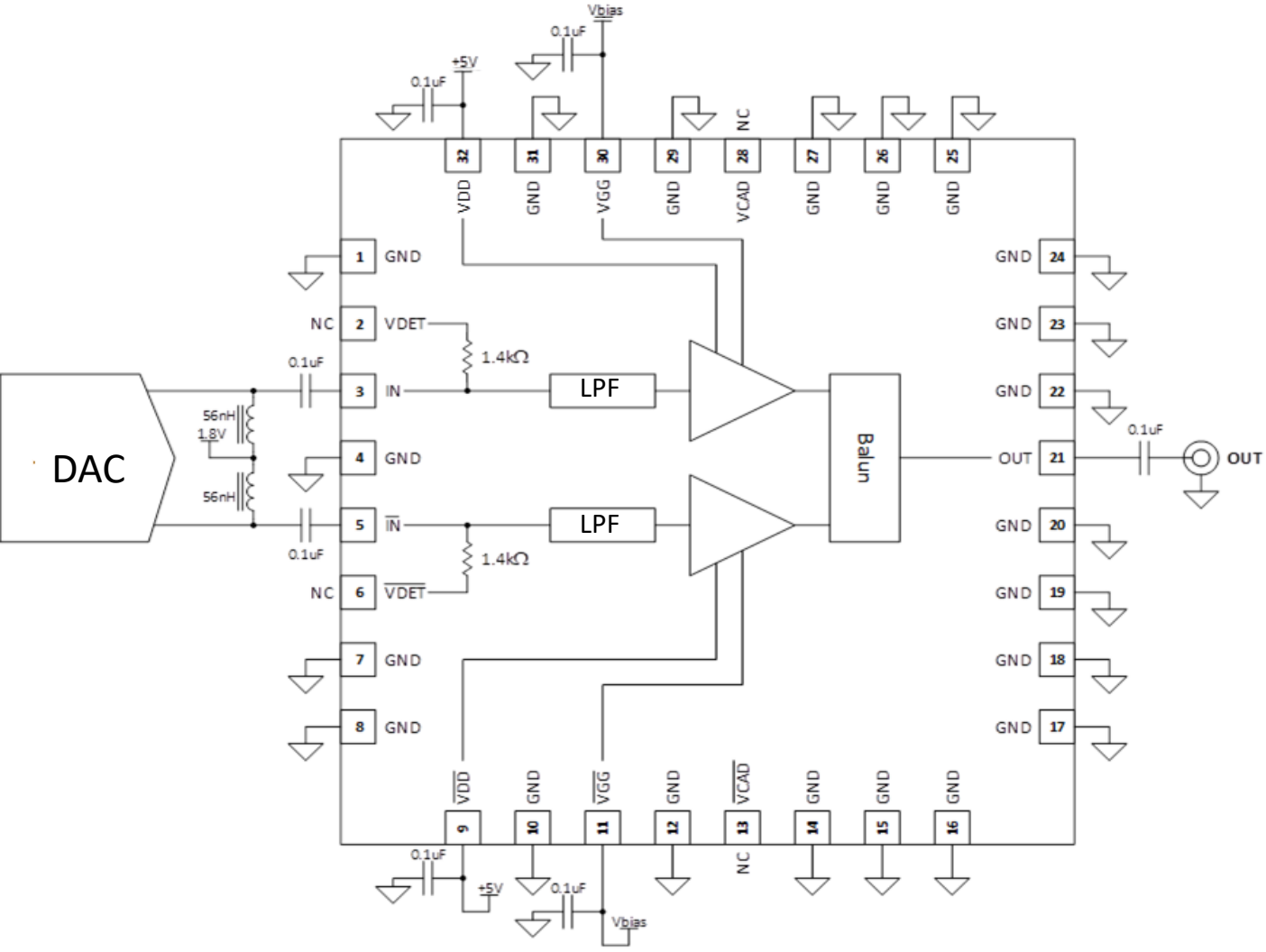


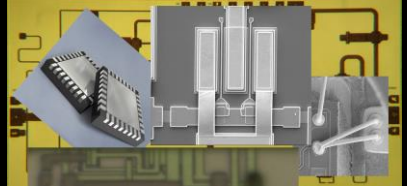
Input and output signals are DC coupled (need to add blocking capacitors)



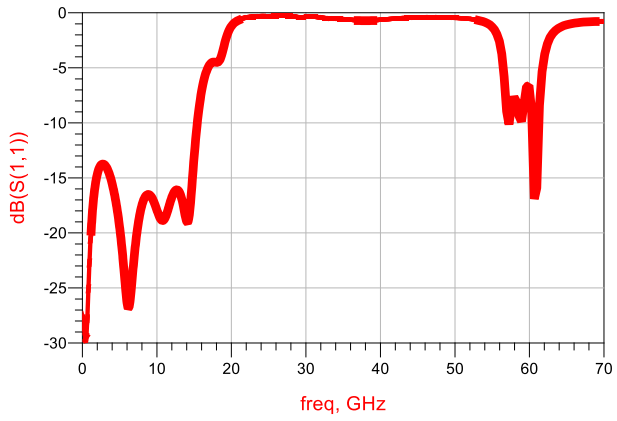
Note: Ceramic Air-cavity or Plastic Overmold package options are also available



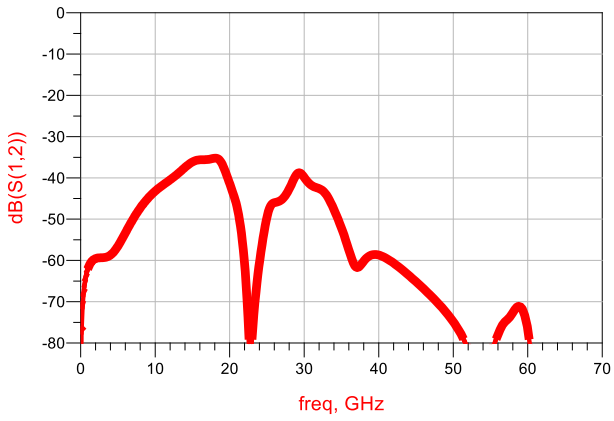

Vbias
0.1uF
+5V
0.1uF
32 VDD
31 GND
30 VGG
29 GND
28 NC VCAD
27 GND
26 GND
25 GND
1 GND
NC 2 VDET
1.4kΩ
0.1uF
3 IN
LPF
56nH
1.8V
56nH
4 GND
5 IN
LPF
0.1uF
1.4kΩ
NC 6 VDET
7 GND
8 GND
Balun
GND 24
GND 23
GND 22
OUT 21
0.1uF
OUT
GND 20
GND 19
GND 18
GND 17
DAC
9 VDD
10 GND
11 VGG
12 GND
13 NC VCAD
14 GND
15 GND
16 GND
0.1uF
+5V
0.1uF
Vbias



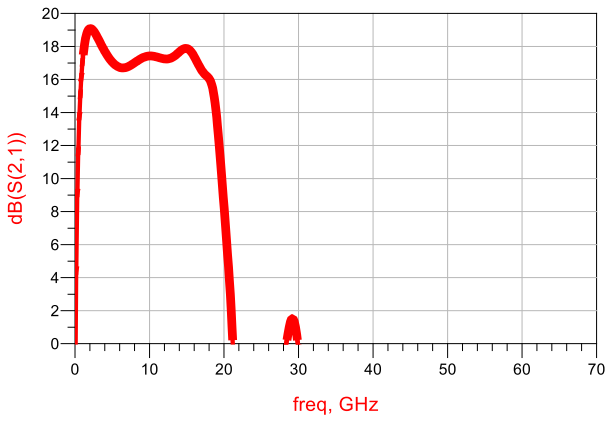
TMC160 Input Return Loss



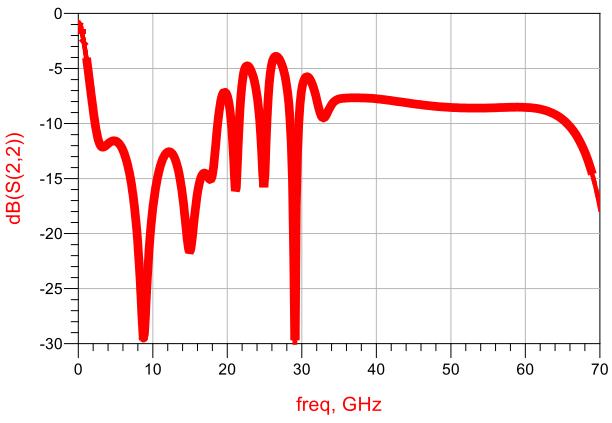
TMC160 Reverse Isolation



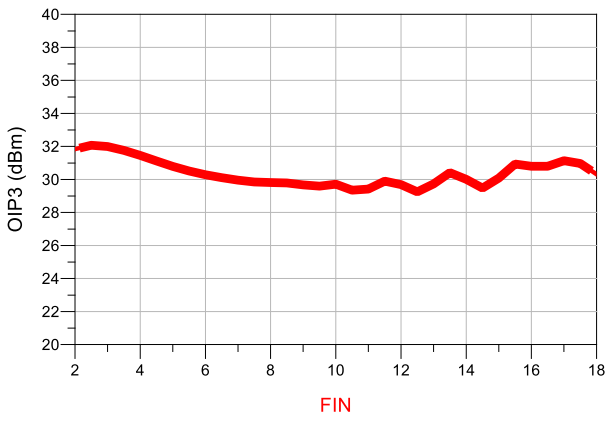
TMC160 Gain



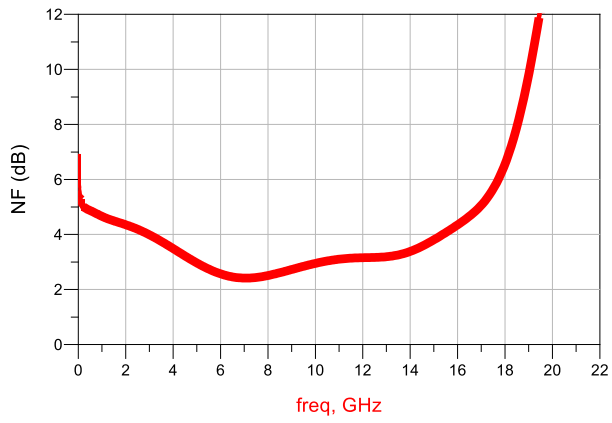
TMC160 Output Return Loss

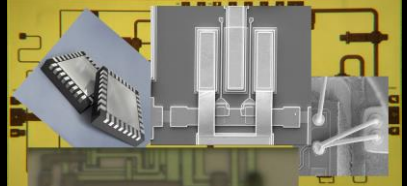


TMC160 OIP3



TMC160 Noise Figure (dB)



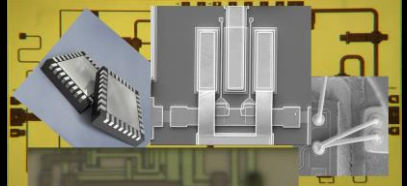


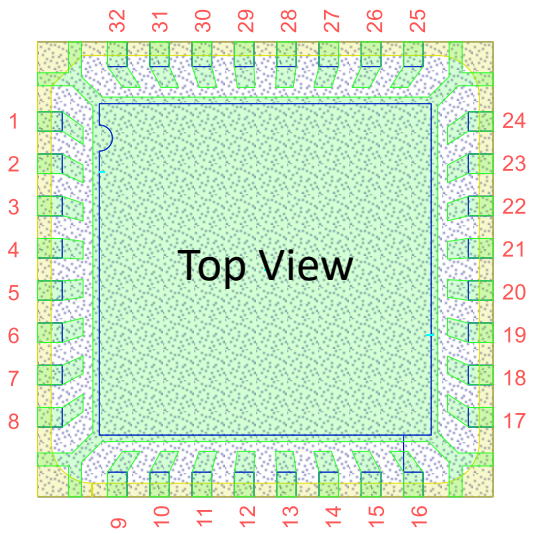
- Recommended Biasing
  - The TMC160-16 is operated with one positive supply VDD (VD1=VD2) and one negative supply voltage VGG (VG1=VG2). The positive supply must be connected to VD1 and VD2 pads on the package. The negative voltage VGG should be connected to VG1 and VG2 pads on the package. The VGG is biased to -1V first, then VDD is gradually biased to +5V and finally, VG1 and Vg2 are adjusted to around -0.7V for ID1=ID2=125mA DC current.
  - Reverse the sequence during power down, i.e. bring the VGG to -1V, lower VDD to 0V, and then VGG to 0.

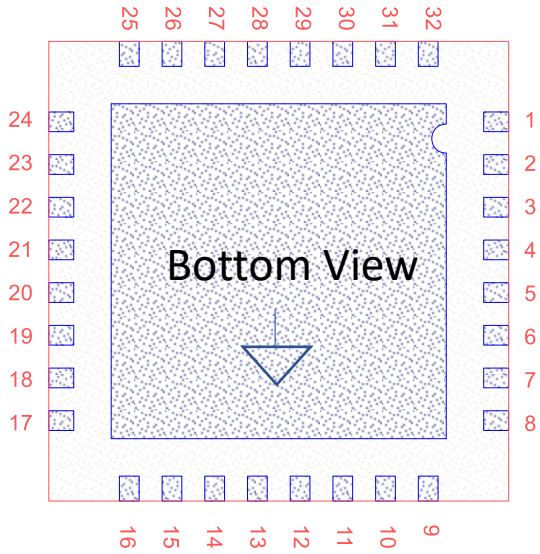
- Assembly Techniques
  - The TMC160-16 is fabricated using a GaAs-based semiconductor material structure and is to be packaged in an air-cavity QFN. The package is back-metalized and can be mounted with standard PCB assembly techniques. The mounting surface should be clean and flat.

- ESD Warning
  - III-V MMICs are ESD-sensitive. Preventative ESD measures must be employed in all aspects of storage, handling, and assembly. MMIC ESD precautions, handling considerations, and die-attach and bonding methods are critical factors in successful III-V MMIC performance and reliability.

- RoHS Compliance
  - This part is RoHS compliant, meeting the requirements of the EU Restriction of Hazardous Substances Directive 2002/95/EC, commonly known as RoHS. Six substances are regulated: lead, mercury, cadmium, chromium VI (hexavalent chromium), polybrominated biphenyls (PBB), and polybrominated biphenyl ethers (PBDE). RoHS compliance requires that any residual concentration of these substances is below the Directive's maximum concentration values (MCV): cadmium 100ppm by weight and all others 1000ppm by weight.







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2	Input Detector Voltage
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6	Input bar Detector Voltage

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21	Output

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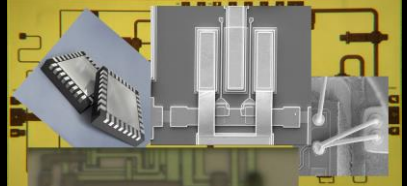
28	VCAD BIAS (Input)
30	VGG BIAS (Input)
32	VDD BIAS (Input)

Leave pins 13 and 28 are internally biased. Leave them open for normal operation. They can be biased externally for fine-tuning the performance.
Pins 2 and 6 are connected with a 1.4KΩ resistor to pins 3 and 5, respectively.
Input and outputs are DC coupled. DC blocking caps are needed, Choose values to adjust the low-frequency end.
Connect all unused pins to GND.



	Absolute Maximum Ratings
Drain Bias Voltage (VDD)	+10V
Gate Bias Voltage (VG1)	-2 to 0V
Gate Bias Current (IG1)	+4mA
RF Input Power (RFIN)(VDD=+8V)	+25 dBm
Channel Temperature	175 °C
Continuous Pdiss (T = 85 °C) (derate 40 mW/°C above 85 °C)	2.5 W
Thermal Resistance (channel to package bottom)	36 °C/W
Storage Temperature	-65 to +150 °C
Operating Temperature for MTTF > 1E6 hours	-55 to +125 °C