mmTron
Unleashing the mmWave Frontier

TMC160-P7
3-16 GHz DAC Interface IC

Product Features

- RF frequency: 3 to 16 GHz
- Linear Gain: 16 dB
- OIP3: 29 dBm
- PKG Size: X=7 mm, Y=7 mm, Z=0.8 mm
- DC Power: 5 VDC, 250 mA

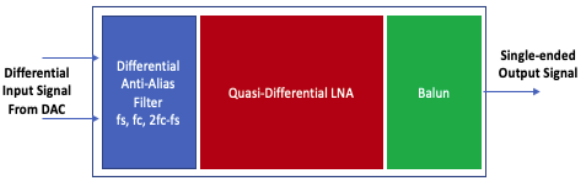
Applications

- Software-Defined Radio
- Instrumentation
- 5G Wireless
- SATCOM
- Military Radar, EW

Product Description

The TMC160-P7 DAC interface low noise quasi differential amplifier consists of a differential anti-alias filter, a pair of quasi differential distributed low noise amplifiers and designed to be integrated with a balun packaged in an air-cavity QFN. TMC160-P7 is designed for use in 5G wireless, SATCOM, Instrumentation and Military Radar and EW applications. The TMC160-P7 is a 50 W matched design with built-in bias-T which eliminates the need for RF port matching and external bias-T. TMC160-P7 can be biased from 5V to 8V and from 125mA to 160mA to optimize Noise Figure and Linearity for a variety of applications. To ensure rugged and reliable operation and moisture protection, the TMC160-P7 is designed and laid out for maximum reliability. Both bond pad and backside metallization are Au-based that is compatible with ribbon and wedge bonding and high conductivity epoxy and eutectic die attach methods. The anti-alias filter can be custom designed to reject clock frequency and its mixing components.

Functional Block Diagram



*Input and Output signals are DC coupled (need to add blocking capacitors)

Ordering Information

Part No.	Description
TMC160-P7	Packaged (Air cavity QFN)
TMC160-PXX	Other Package Options[1]

1- Also available ceramic air-cavity or plastic overmold.

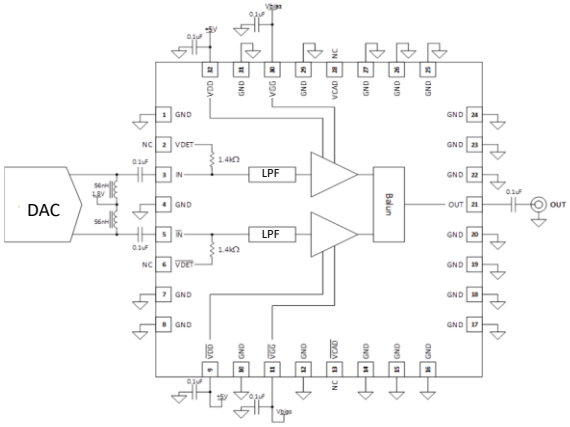
Table of Contents

Product Description……...……..……..1
Product Features……...……....1
Functional Block Diagram…….....1
Applications…….....1
Ordering Information……...1
Typical Operating Conditions..…….....2
Schematic TMC160……...……..…2
Input Return Loss, TMC160...…….....3
Reverse Isolation, TMC160...……...……3
Gain, TMC160...……3
Output Return Loss , TMC160……..3
OIP3, TMC160……..……...3
Noise Figure, TMC160……..……3
Power up and Bias Sequencing……..……..…4
Packaged Device Layout Drawing……4
Pad/Pin Location and Functional Description.....4
Recommended Biasing……..…..…5
Assembly Techniques……..…5
Absolute Maximum Ratings……...6
ESD Warning…….…….....7
ROHS Compliance……..….....…7
Disclaimer…….....8

Typical Operating Conditions

	Min	Typ	Max	
Frequency	3		16	GHz
Gain		16		dB
Noise Figure		4		dB
OIP3		29		dBm
Return Loss		10		dB
Bias Voltage		5		V
Bias Current		250		mA

Schematic TMC160



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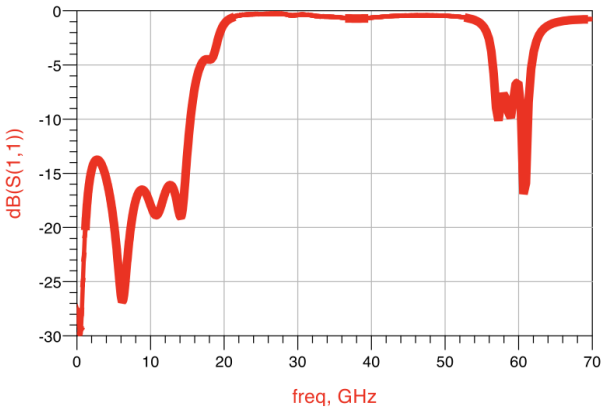
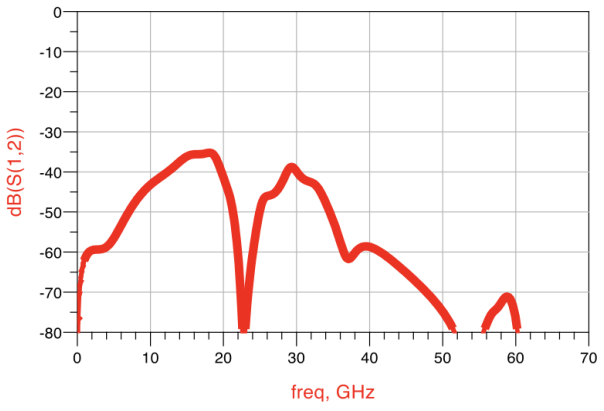
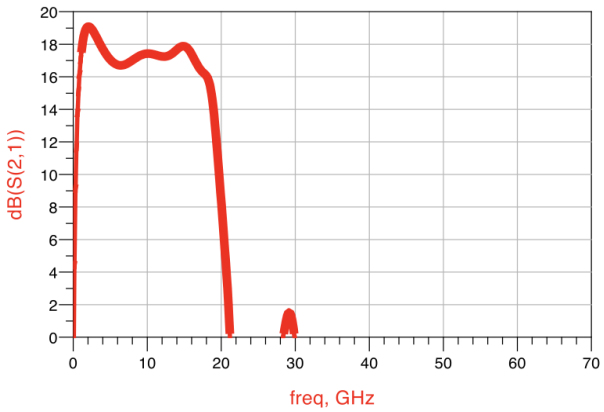
TMC160 Input Return Loss



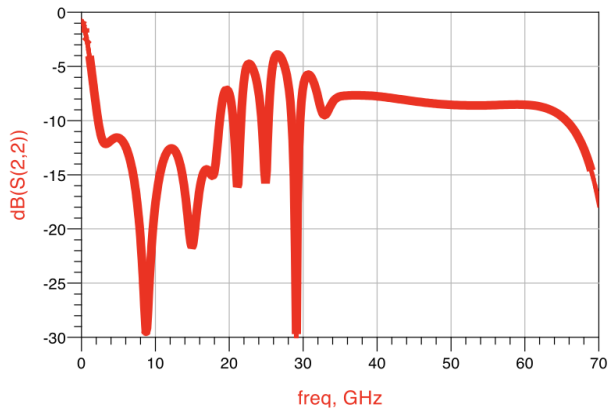
TMC160 Reverse Isolation



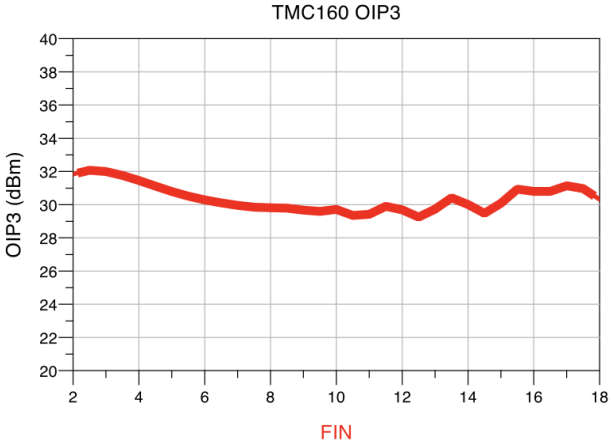
TMC160 Gain



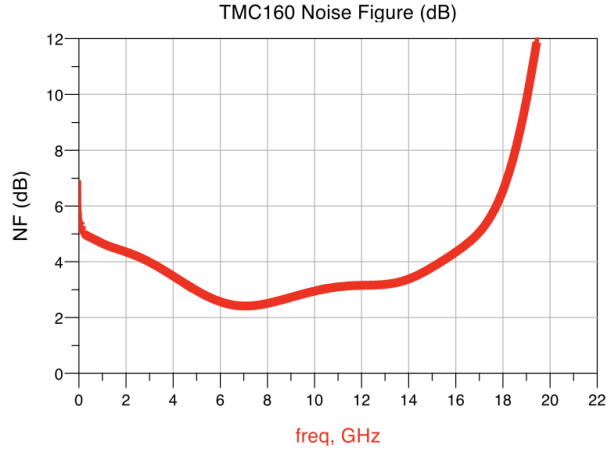
TMC160 Output Return Loss



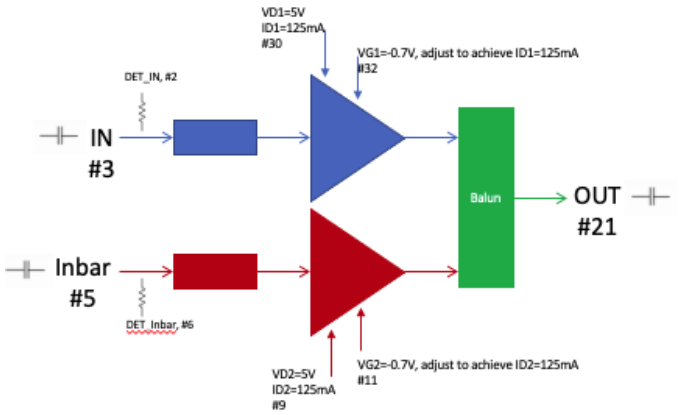
TMC160 OIP3



TMC160 Noise Figure (dB)

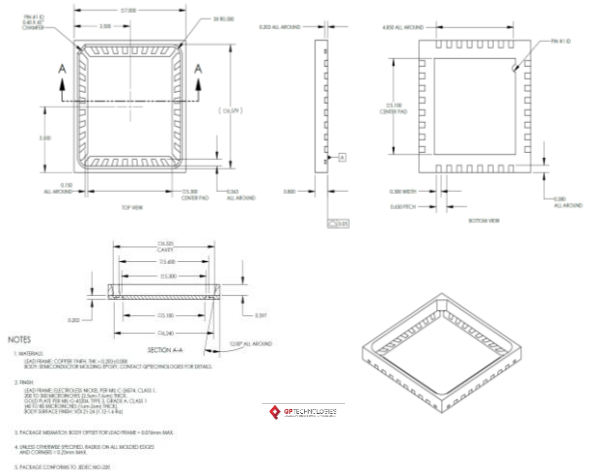


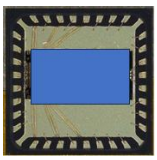
TMC160 Power Up and Bias Sequencing



Bias Sequencing: To turn ON the device, VG1, and VG2 are first set at -1V. Then set VD1 and VD2 to 5V. Finally, adjust VG1 and VG2 to achieve ID1=ID2=125mA. To turn OFF the device, you set VG1 and VG2 to -1V, then turn off the VD1 and VD2 followed by turning off VG1 and VG2.

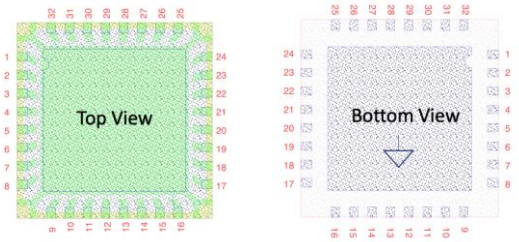
TMC160 Pad/Packaged Device Layout Drawings





Pin/Pad#	Function
2	Input Detector Voltage
3	Input
4	GND
5	Input /
6	Input Detector Voltage /

Pin/Pad#	Function
9	VDD Bias (Input /)
11	VGG Bias (Input /)
13 (*)	VCAD Bias (Input /)
20	GND
21	Output



Pin/Pad#	Function
22	GND
28 (*)	VCAD Bias (Input)
30	VGG Bias (Input)
32	VDD Bias (Input)

(*) Pins 13 and 28 are internally biased. Leave them open for normal operation. They can be biased externally for fine-tuning the performance.

- Pins 2 and 6 are connected with a 1.4K Ohm resistor to pins 3 and 5, respectively.
- Input and outputs are DC coupled. DC blocking caps are needed, Choose values to adjust the low-frequency end.
- Connect all unused pins to GND.

Recommended Biasing

The TMC160-P7 is operated with one positive supply VDD (VD1=VD2) and one negative supply voltage VGG (VG1=VG2). The positive supply must be connected to VD1 and VD2 pads on the package. The negative voltage VGG should be connected to VG1 and VG2 pads on the package. The VGG is biased to -1V first, then VDD is gradually biased to +5V and finally, VG1 and Vg2 are adjusted to around -0.7V for ID1=ID2=125mA DC current.

Reverse the sequence during power down, i.e. bring the VGG to -1V, lower VDD to 0V, and then VGG to 0.

Assembly Techniques

The TMC160-P7 is fabricated using a GaAs-based semiconductor material structure and is to be packaged in an air-cavity QFN. The package is back-metalized and can be mounted with standard PCB assembly techniques. The mounting surface should be clean and flat.

Absolute Maximum Ratings

Parameter	Value / Range
Drain Bias Voltage (VD)	+10 V
Gate Bias Voltage (VG1)	-2 to 0 V
Gate Bias Current (IG1)	+4 mA
RF Input Power (RFIN) (VDD=+8V)	+25 dBm
Channel Temperature	175 °C
Continuous Pdiss (T= 85°C) (Derate 40 mW/°C above 85 °C)	2.5 W
Thermal Resistance (channel to package bottom)	36 °C/W
Storage Temperature	-66 to +150 °C
Operating Temperature for MTTF>1E6 hrs.	-55 to +150 °C

NOTE: Operation of TMC160 outside the parameter ranges given above can cause irreversible damage.



Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. mmTron Inc. recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications. III-V MMICs are ESD-sensitive. Preventative ESD measures must be employed in all aspects of storage, handling, and assembly. MMIC ESD precautions, handling considerations, and die-attach and bonding methods are critical factors in successful III-V MMIC performance and reliability.



RoHS Compliant

This part is RoHS compliant, meeting the requirements of the EU Restriction of Hazardous Substances Directive 2002/95/EC, commonly known as RoHS. Six substances are regulated: lead, mercury, cadmium, chromium VI (hexavalent chromium), polybrominated biphenyls (PBB), and polybrominated biphenyl ethers (PBDE). RoHS compliance requires that any residual concentration of these substances is below the Directive's maximum concentration values (MCV): cadmium 100ppm by weight and all others 1000ppm by weight.

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